**Synchronous counters**

**Lab no #12**

** Fall 2019**

**Fall 2021**

**CSE202L Digital logic and computer design**

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Class Section: **B**

“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

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**OBJECTIVES**

After completing this experiment, you will be able to: 

* Analyze the count sequence of a synchronous counter.
* To design and implement 3 bit synchronous up/down counter.

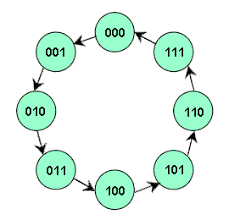
**COMPONENTS REQUIRED** 

* Two 7476, JK flip flop ICs 
* One 7411, 3 I/P AND gate 
* One 7432, 2 I/P OR gate 
* One 7486, 2 I/P XOR gate 
* One 7404, hex inverter

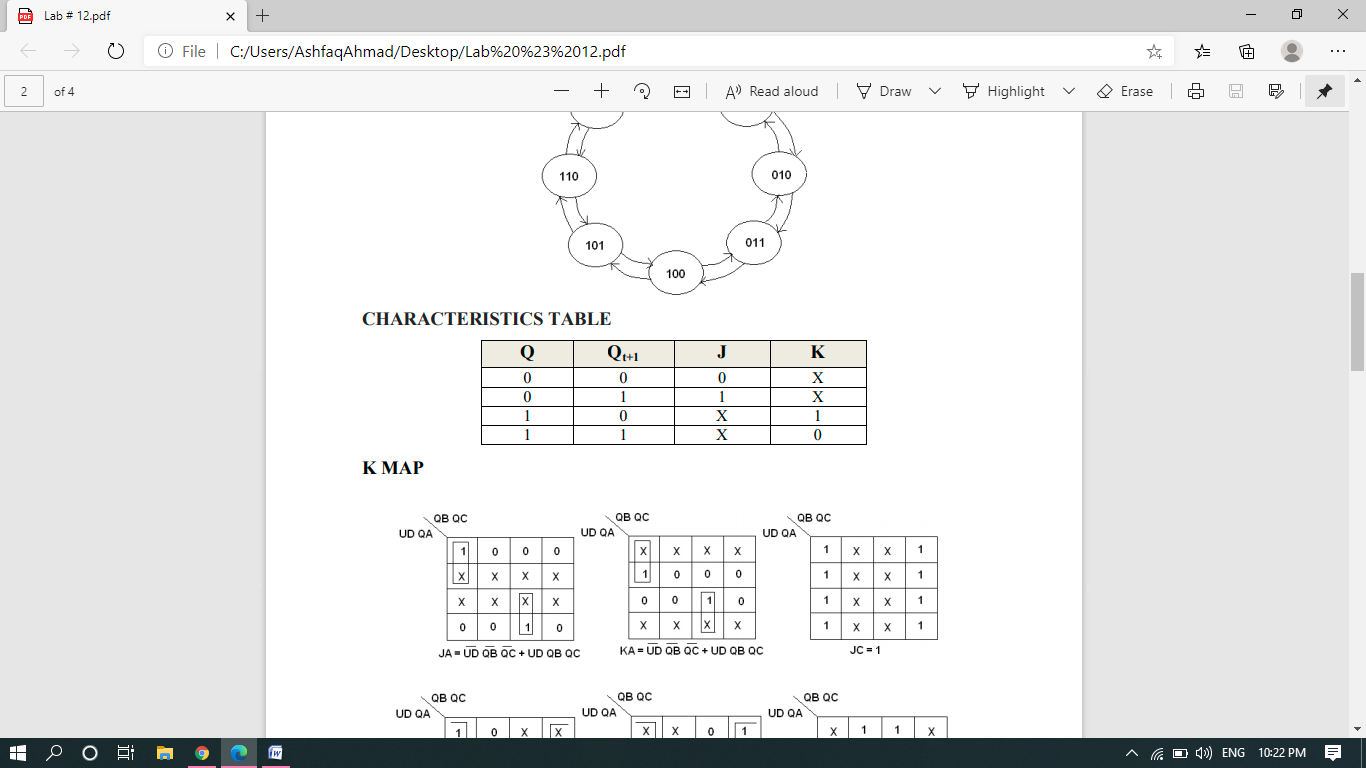
**THEORY:**

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. Synchronous counters have all clock lines tied to a common clock, causing all flip-flops to change at the same time. For this reason, the time from the clock pulse until the next count transition is much faster than in a ripple counter. This greater speed reduces the problem of glitches (short, unwanted signals due to non-synchronous transitions) in the decoded outputs. However, glitches are not always eliminated, because stages with slightly different propagation delays can still have short intermediate states. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

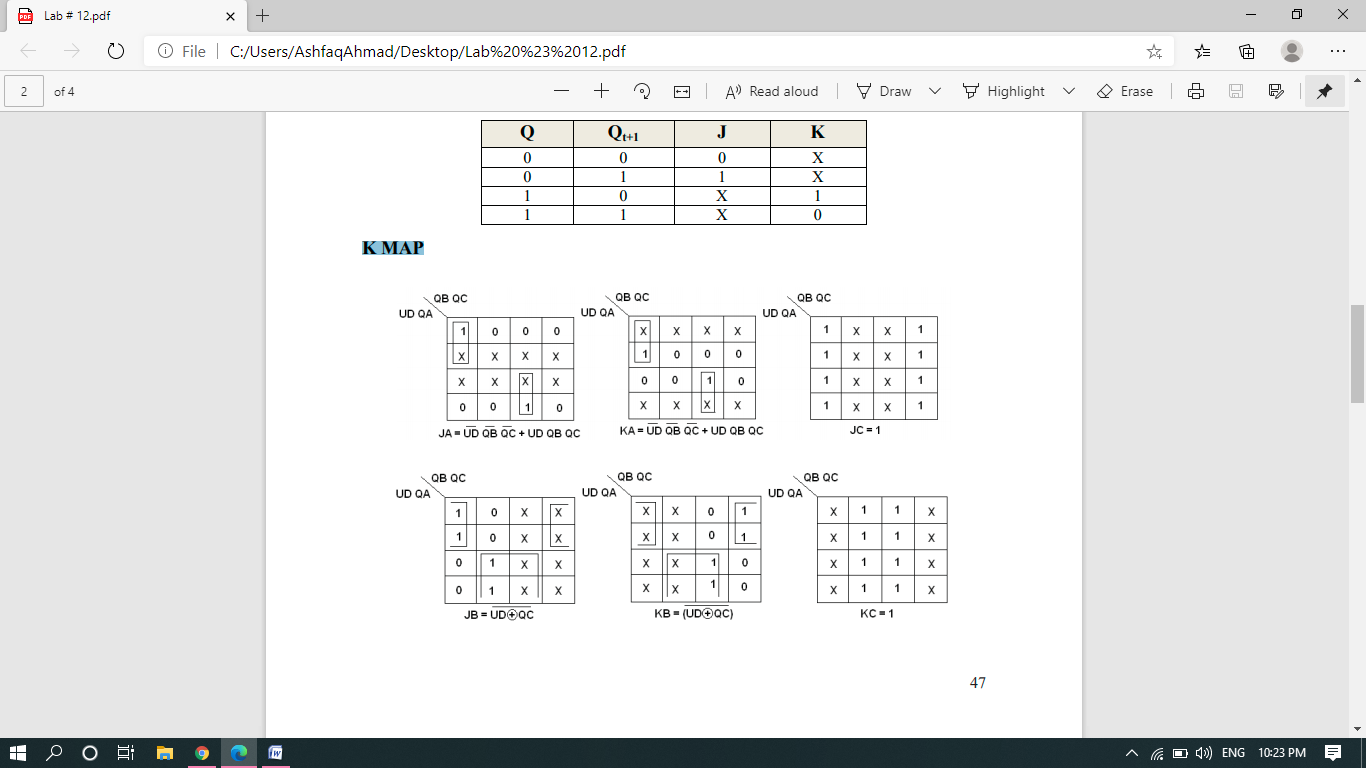
**State Diagram:**

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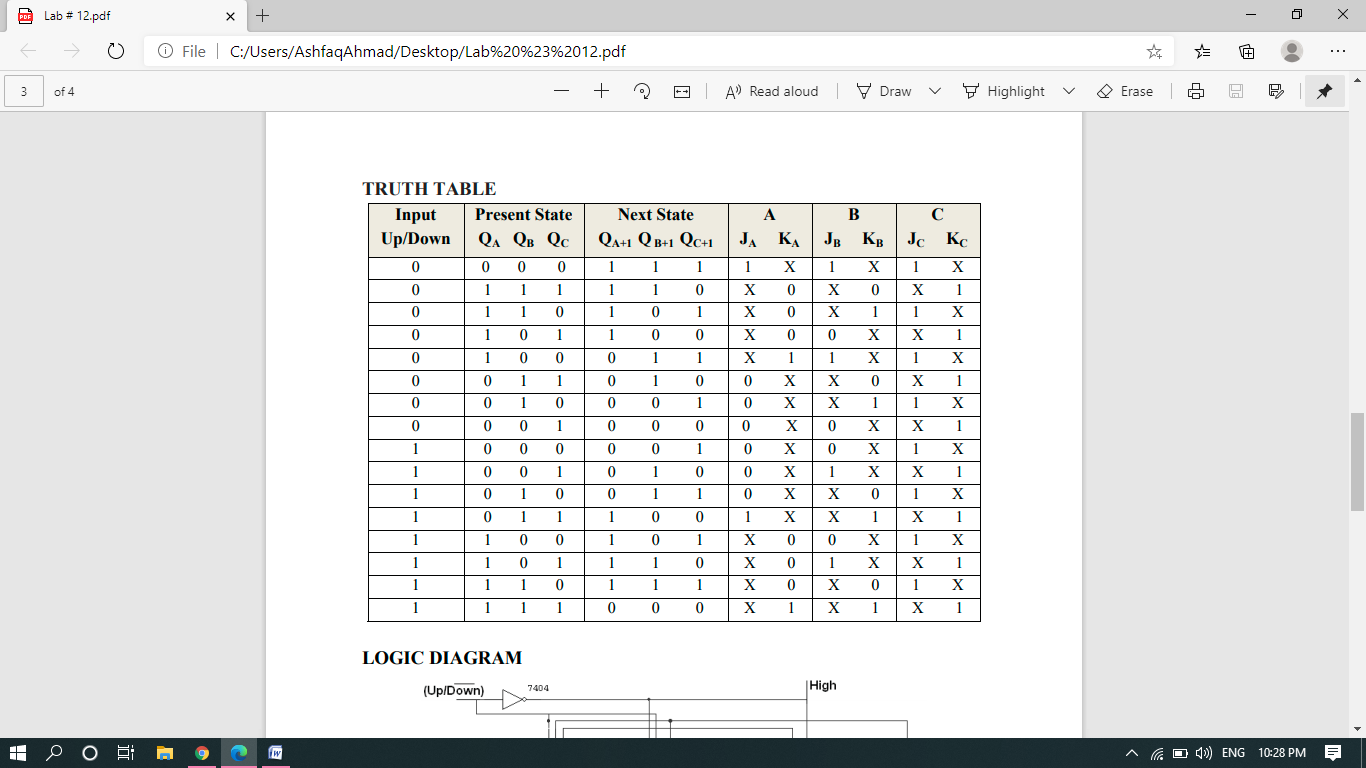
CHARACTERISTICS TABLE

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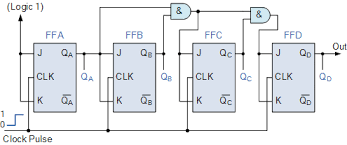
**K-MAP:**

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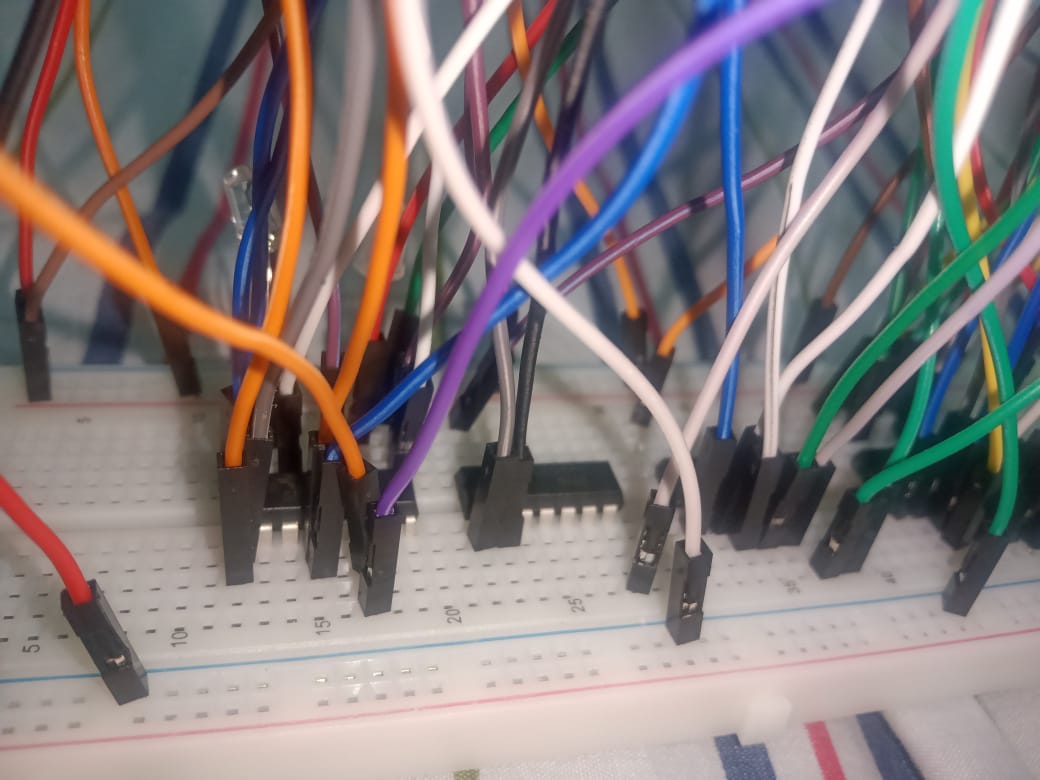
**TRUTH TABLE:**

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**4-Bits Synchronous Counter:**

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**Real Life Picture:**

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**PROCEDURE **

* Connections are given as per circuit diagram. 
* Logical inputs are given as per circuit diagram. 
* Observe the output and verify the truth table.

**REVIEW QUESTIONS**

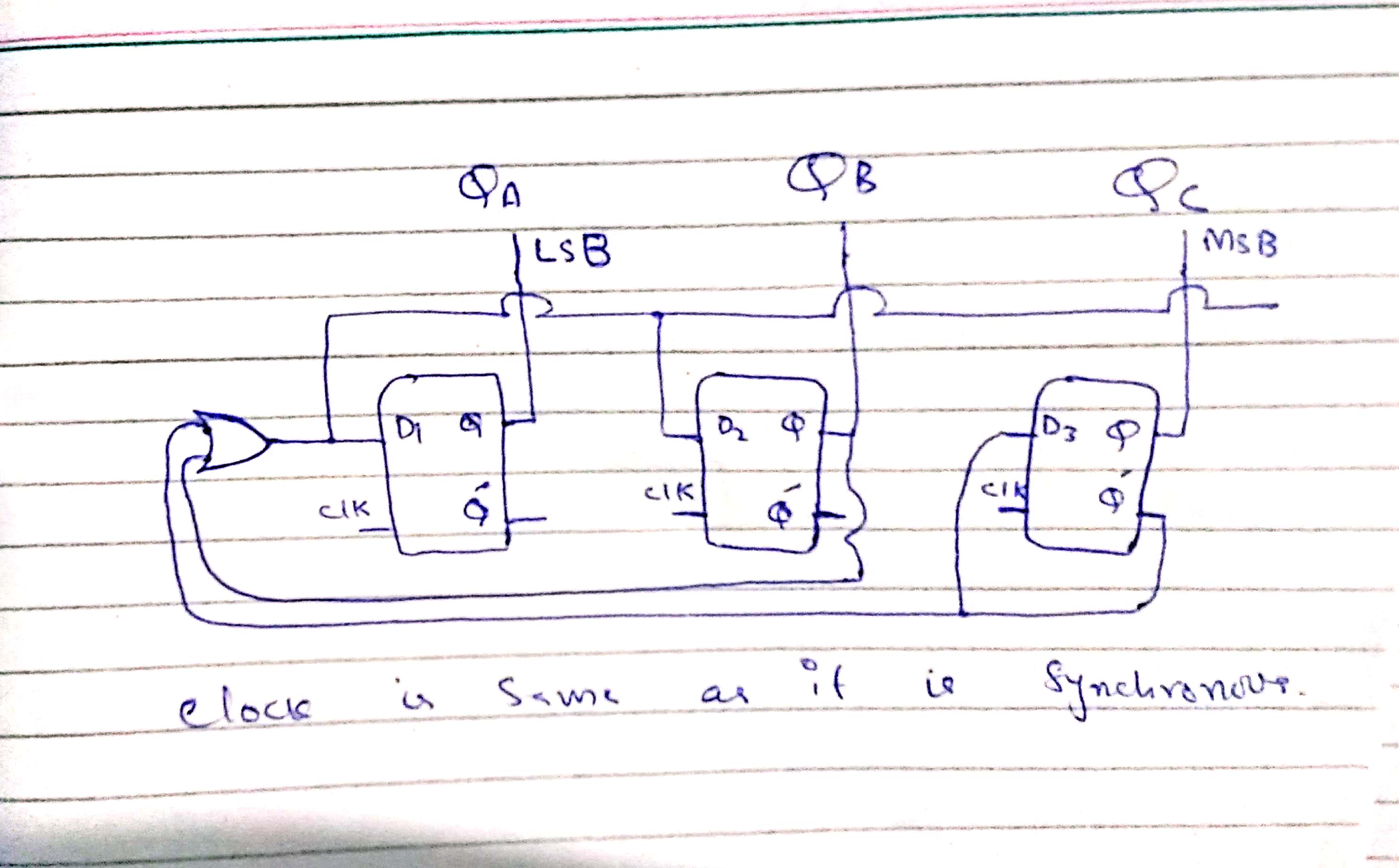
1. What is the difference between asynchronous and synchronous counters? Which counter will you prefer to use in your circuits and why? Also specify the main drawbacks of asynchronous counters.

**Answer:**

1. **Synchronous counter** is the one in which all the flip flops are clocked simultaneously with the similar clock input. On the contrary, an **asynchronous counter** is a device in which all the flip flops that constitute that **counter** are clocked with different input signals at different instants of time.
2. **Asynchronous counters** are easier to design than **synchronous counters**. are all clocked together at the same time with the same clock signal. Due to this common clock pulse all output states switch or change simultaneously. ... Overall faster operation may be achieved compared to **Asynchronous counters**.
3. Drawbacks:

* An extra “re-synchronizing” output flip-flop may be required.
* To count a truncated sequence not equal to 2n, extra feedback logic is required.
* Counting a large number of bits, propagation delay by successive stages may become undesirably large.
* This delay gives them the nickname of “Propagation Counters”.
* Counting errors occur at high clocking frequencies.
* Synchronous Counters are faster and more reliable as they use the same clock signal for all flip-flops.

1. Design a synchronous counter which counts the sequence 0, -1, -2, -3 using D-flip flops. List all steps.



3) Draw the timing diagram for each flip flop output in part 2.

